REMARKS

By the present amendment and response, independent claims 1, 7, and 23 and dependent claims 4-5, 9-11, 14 and 15 have been amended to overcome the Examiner's objections and claims 6 and 12 have been canceled. Thus, claims 1, 4-5, 7, 9-11, 14-15, and 23 remain pending in the present application. Reconsideration and allowance of pending claims 1, 4-5, 7, 9-11, 14-15, and 23 in view of the following remarks are requested.

The Examiner has rejected claims 7, 9-12, and 14-15 under 35 USC §112, first paragraph. Applicant has amended claims 7, 9-11, and 14-15 and canceled claim 12 in response to the Examiner's objection and submits that the requirements of 35 USC §112, first paragraph, have been met.

The Examiner has further rejected claims 6-7, 9-12, and 14-15 under 35 USC §112, second paragraph. Applicant has amended claims 7, 9-11, and 14-15 and canceled claims 6 and 12 in response to the Examiner's objection and submits that the requirements of 35 USC §112, second paragraph, have been met.

The Examiner has further rejected claims 1, 5-7, 9, 11-12, 14-15, and 23 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,033,956 to Shye-Lin Wu ("Wu") or U.S. patent number 4,713,142 to Mitchell et al. ("Mitchell") in view of U.S. patent number 4,613,956 to Paterson et al. ("Paterson") and "Applicant's admitted prior art." For the reasons discussed below, Applicant respectfully submits that the present

invention, as defined by amended independent claims 1, 7, and 23, is patentably distinguishable over Wu, Mitchell, Paterson, or any combination thereof.

The present invention, as defined by amended independent claims 1, 7, and 23, teaches, among other things, depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer."

As disclosed in the patent application, by forming an insulator layer over a floating gate, where the insulator comprises a high quality oxide, such as a LPCVD furnace grown oxide, the present invention advantageously prevents charge from leaking out vertical side surfaces of the float gate. Also, as disclosed in the present application, after the insulator layer has been deposited, the insulator layer is polished using chemical-mechanical polishing technique until a thickness of a second region of the insulator layer is substantially equal to a thickness of the floating gate. As a result, the present invention achieves a level, planar layer comprising the floating gate and the insulator layer, which advantageously provides a level surface on which an ONO layer and a control gate layer can be subsequently deposited.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Wu does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer." Wu specifically discloses depositing CVD TEOS oxide 210 over polysilicon layer 204 and polysilicon slots 205, spinning planarizing photoresist 212 on the wafer, applying a second resist coat, and utilizing a planarizing plasma etch to etch both CVD TEOS oxide layer 210 and photoresist 212 such that the surface of polysilicon layer 204 is exposed. See, for example, Wu, column 1, lines 46-58. However, Wu fails to teach, disclose, or suggest an insulating layer comprising a high temperature oxide or a high quality oxide that is formed by an LPVCD process. Furthermore, Wu fails to teach, disclose, or suggest polishing the insulator layer immediately after insulator layer has been deposited. In Wu, after CVD TEOS oxide layer 210 is deposited, two photoresist coats are applied and a planarizing plasma etch is utilized to etch both CVD TEOS oxide layer 210 and photoresist 212.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Mitchel does not teach, disclose, or suggest depositing an insulator layer

comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer." Mitchel specifically discloses subjecting polycrystalline silicon layer 33 and gate oxide layer 32, which are formed on the surface of substrate 1, to a thermal oxidation to form silicon dioxide layer 36. See, for example, column 2, lines 64-68, column 3, line 1, and Figure 2b of Mitchel. In Mitchel, silicon dioxide layer 37 is then formed by chemical vapor deposition on silicon dioxide layer 36, photoresist layer 38 is formed over silicon dioxide layer 37, and an anisotropic etching process is utilized to etch photoresist layer 38 and silicon dioxide layer 37. See, for example, column 3, lines 8-19 and Figures 2c and 2d of Mitchel. Thus, in Mitchel, silicon dioxide layer 36 is situated between silicon dioxide layer 37 and polycrystalline silicon layer 33 and gate oxide layer 32.

Thus, Mitchel fails to teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, where the insulator layer is deposited to a thickness greater than the thickness of the floating gate. Additionally, Mitchell fails to teach, disclose, or suggest an insulator layer formed in a LPCVD process. Furthermore,

Mitchell fails to teach, disclose, or suggest polishing the insulator layer immediately after the insulator layer has been deposited.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Paterson does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer." Paterson specifically discloses performing all depositions in LPCVD processes in a tube reactor such that the amount of thermal cycling of the tube reactor is kept to an absolute minimum to avoid undesirable particulate release. See, for example, Paterson, column 5, lines 22-35. However, Paterson fails to teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer."

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, and 23, is not suggested, disclosed, or taught by Wu, Mitchell, and Paterson, singly or in any combination thereof. As such, the present invention, as defined by amended independent claims 1, 7, and 23, is patentably distinguishable over Wu, Mitchell, and Paterson. Thus claim 5 depending from amended independent claim 1 and claims 9, 11, and 14-15 depending from amended independent claim 7, are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 4 and 10 under 35 USC §103(a) as being unpatentable over Wu or Mitchell taken with Paterson and "Applicant's admitted prior art," and further in view of U.S. patent number 5,808,339 to Yamagishi et al. ("Yamagishi") and "Applicant's admitted prior art." As discussed above, amended independent claims 1 and 7 are patentably distinguishable over Wu, Mitchell, and Paterson and, as such, claim 4 depending from amended independent claim 1 and claim 10 depending from amended independent claim 7 are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 1, 4-7, 9-12, 14-15, and 23 under 35 USC §103(a) as being unpatentable over Yamagishi or U.S. patent number 6,051,467 to Chan et al. ("Chan") taken with "ULSI Technology," p. 211, by Sze et al. ("Sze") and in

view of "Applicant's admitted prior art." For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, and 23, is patentably distinguishable over Yamagishi, Chan, Sze, or any combination thereof.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Yamagishi does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. Yamagishi specifically discloses electrode pattern 53 formed over first gate insulating layer 51 and second insulating layer 54 formed over electrode pattern 53 and element isolation region 13, where insulating layer 54 is formed by a CVD method. See, for example, column 12, lines 11-30 and Figures 9A-9E. In Yamagishi, first gate insulating layer 51 is situated only under electrode pattern 53. Thus, in Yamagishi, insulating layer 54 is not formed directly on first gate insulating layer 51 (i.e. a tunnel oxide layer) as required in amended independent claims 1, 7, and 23. Furthermore, Yamagishi fails to teach, disclose, or suggest forming insulating layer 54 in a LPCVD process.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Chan does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a

tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. Chan specifically discloses depositing oxide layer 30 over substrate 10 that includes floating polysilicon gate 18, which is situated between sidewall spacers 24 and over gate oxide layer 16. See, for example, column 3, lines 10-22 and Figures 2-4 of Chan. In Chan, oxide layer 30 is formed on the top surface of substrate 10, on sidewall spacers 24, and on the top surface of floating polysilicon gate 18. Thus, in Chan, as a result of sidewall spacers 24, oxide layer 30 is not in contact with vertical surfaces of floating polysilicon gate 18 or directly on gate oxide layer 16. Furthermore, Chan fails to teach, disclose, or suggest an insulator layer formed by a LPCVD process.

In contrast to the present invention as defined by amended independent claims 1, 7, and 23, Sze does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. Sze is cited by the Examiner to disclose the advantages provided by a dielectric layer formed by using a LPCVD process. However, Sze does not teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with

vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, and 23, is not suggested, disclosed, or taught by Yamagishi, Chan, and Sze, singly or in any combination thereof. As such, the present invention, as defined by amended independent claims 1, 7, and 23, is patentably distinguishable over Yamagishi, Chan, and Sze. Thus claims 4-5 depending from amended independent claim 1 and claims 9-11 and 14-15 depending from amended independent claim 7, are, *a fortiori*, also patentably distinguishable over Yamagishi, Chan, and Sze for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 7, and 23 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 8/20/03

Michael Farjami, Esq.
Reg. No. 38, 135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: 8/20/03

Lori Llave
Name of Person Mailing Paper and/or Fee

Lori Llave 8/20/03
Signature Date